Cross-Coupled Charge Pump Synthesis Based on Full Transistor-Level

Jan MAREK[1], Jiri HOSPODKA[1], Ondrej SUBRT[1,2]

[1]Department of Circuit Theory, Faculty of Electrical Engineering, Czech Technical University in Prague,
Technicka 2, 160 00 Prague, Czech Republic
[2]ASICentrum, a Company of the Swatch Group,
Novodvorska 994, 142 00 Prague, Czech Republic

marekj20@fel.cvut.cz, hospodka@fel.cvut.cz, ondrej.subrt@asicentrum.cz

Abstract. *This paper presents utility for the design of the cross-coupled charge pump, which is used for supplying peripherals with low current consumption on the chip, as the EEPROM or FLASH memories. The article summarizes the knowledge in the field of the theoretical and practical analysis of the cross-coupled charge pump (design relationships and their connection with the pump parameters, as the threshold voltage, power supply voltage, clock signal frequency, etc.) that are applicated in the design algorithm. Optimal MOSFETs sizes (W, L) were find based on the construct of the time response characteristics of the pump sub-block and finding of the maximal voltage increase in the active interval of the clock signal and minimizing of the pump losses, as the switch reverse current, inverter cross current, etc. Synthesis process includes the design of the pump functional blocks with dominant real properties, which are described based on BSIM equations for long channel MOSFET. The pump stage complex model is applicated for estimation of the number of pump stages via state-space model description and using of the interpolation polynomial functions in the algorithm. It involves the construction of the time response characteristic due to the state variables and prediction of the number of the pump stages for the next cycle based on the previous data. Optimization of the pump area is based on the minimizing of the main capacitor in each of the pump stages (number of the pump stages must be increased to obtain the desired output voltage value). Access is designed to stress the maximum pump voltage efficiency. The whole procedure is summarized in the practical example, in which the solution is shown both in terms of maximal voltage efficiency and the optimal pump area on a chip with respect to the clock signal frequency. Added functions of the design environment are explained, inclusive of the designed pump netlist generating for professional design environment Mentor Graphics including the real models of components that are available in library MGC Design Kit. The procedure gives designer credible results without long time-consuming optimization process. In addition, the complex model allows the inclusion effects of higher-levels.*

Keywords

1. Introduction

Cross-coupled charge pump represents the advanced concept of two-phase SC circuits that are an alternative way to classical DC/DC boost converters, see Fig. 1. An effective pump area of the chip represents one of the main advantages of the voltage converters without inductors. Moreover, the mentioned structure allows achieving high pump efficiency while the circuit structure remains relatively simple. On contrary, some types of the modern charge pump require a multiphase clock signal so that the strict requirements for the driving circuit are inevitable. Charge pumps fall into the category quasi-analogue circuits from the view of the signal processing. Circuit topology was detailed analyzed in many publications [1], [2], [3], [4] and [5] and sizing of its components were recommended to achieve the maximal voltage gain, static efficiency respectively:

$$\varepsilon_v = \frac{V_{out,av}}{(N+1)V_{DD}},\qquad(1)$$

where $V_{out,av}$ is the average value of the output voltage in (V), N is the number of stages and V_{DD} is supply
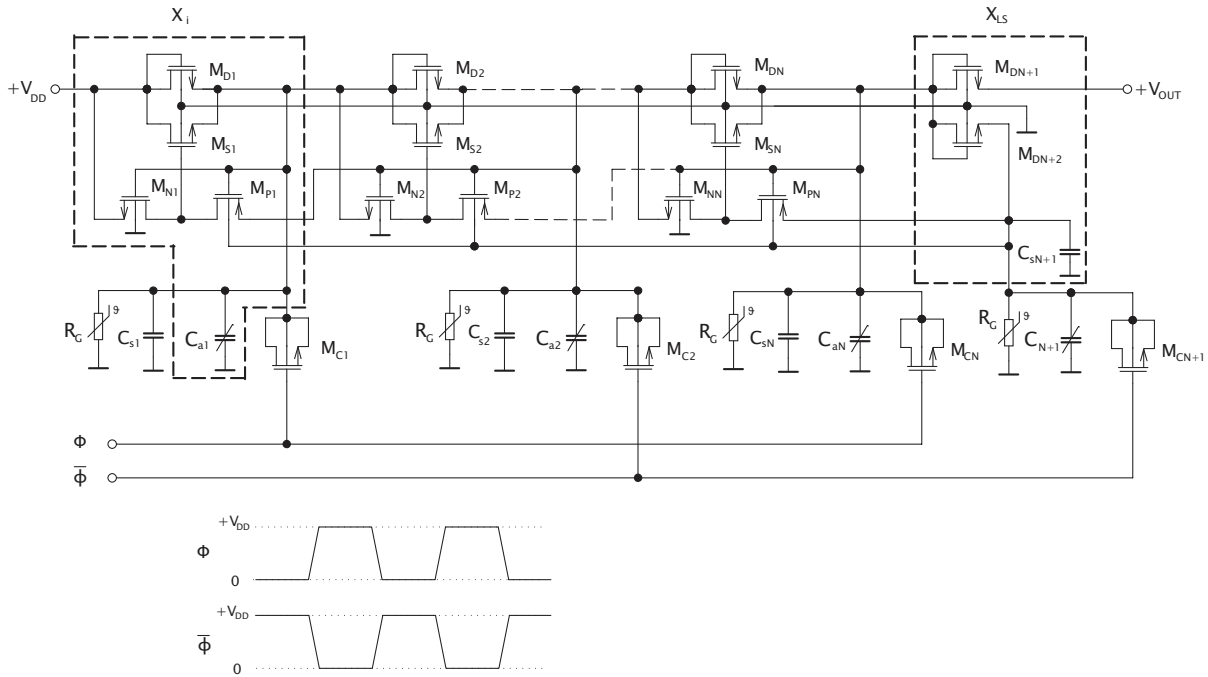
Fig. 1: Cross-coupled charge pump diagram implemented with MOS capacitors and parasitic impedances.

voltage in (V). The design environment for the synthesis of the cross-coupled charge pump will be presented in this paper. The charge pump draft is divided into two basic steps, as the outcome of the current research on the issue: **Design of the pump partial blocks** and **application of the state-space model to determine the number of stages** at the input requirements. Access specification is conceived somewhat nontraditional compared to the known methods for the SC circuits description [2]. Design of the pump functional blocks, labelled X_i and X_{LS} in Fig. 1, is based on the fact that the charge pump has properties of the analogue circuit during phase of the clock signal [2] (analogue part of the model) and transition to the next phase of CLK has discontinuous character in time (digital part-state model). The pump stage blocks are modelled by using the BSIM model equations [6], whose the original form [7] was simplified for this purpose. Complex model of the pump stage, which includes both the static and dynamic part (Ward's capacitance model) is described via the piecewise model [3], [6] and [8] for high-voltage application, where long channel [6] and [9] and strong inversion region of the MOSFETs are expected due to the correct function [2], [4] and [10].

The main part of the article deals with the synthesis process from the design of the functional blocks to the application of the state-space model for finding the number of the stages. One of the main reason for its use is still an unknown relationship between the number of the pump stages and pump output voltage [1] and [4], $V_{out,av} = f(N)$, which would consist properties of the

real structure. The state model was originally used for estimation of the pump properties [11]. Implementation of the new version of the state-space model and some properties of the design environment will be introduced for predicting the number of the pump stages under condition Eq. (1). The synthesis process is demonstrated in the practical example, where the calculation is done in two ways, firstly, to achieve the maximal voltage gain, secondly, minimization of the pump area on a chip. The achieved results are compared with the simulation results of the real structure in the professional simulator. Programme procedure was created in Maple SW and results were verified in Mentor Graphics Design Architect-IC v2008.2_16.4.

The main benefit is the charge pump design utility that allows analogue designers step-by-step synthesis without long-time simulation and numerical optimization process. The internal model is also is universally applicable in terms of both the parameters (model parameters, temperature effects, . . .) and the used MOSFET technology, like PSP or EKV [9] and [12].

2. Synthesis Process

The synthesis process use models and description of the pump circuits presented in [3], [6], [8], [10] and [11]. The charge pump draft is divided into two basic steps, as the outcome of the current research on the issue: *Design of the partial pump blocks* and *finding number of the pump stages* at the input requirements.

Important insights from the block design draft will be summarized in a nutshell. Each block of the pump is designed so that the pump losses [2] would be minimal. The design is based on the analysis of the elementary subcircuit in a configuration, that can occur in the real circuit. Typically, this is a calculation of the time response characteristic, when the clock signal changes the logic level, i.e. state description. Sizing of the components (switch and diode MOSFETs width [3] and [8], main capacitor value [3], ...) is set, so that the result characteristic(s) met the required criterion. A slightly different approach was applied to the CMOS inverter design [6] compared to a design for a digital circuit [9]. The principle of the draft is based on the shifting *inverter switching point* to *down limit*, where one of the MOSFET is at the cut-off border [6]. As the result, it is recommended to keep the ratio between NMOS and PMOS sizes (width and length), $R = \frac{W_n}{L_n} \cdot \frac{L_p}{W_p}$, where R was determined from the sensitivity analysis [6]. Absolute dimensions are designed to satisfy the dynamic properties-propagation delay, which affects the dynamic power dissipation [1]. For calculation of the time delay t_{HL} and t_{LH} is necessary to estimate the inverter load capacitance value, labeled $C_{L_{inv}}$ [13] and [14]. Using the pump capacitance model [8], the inverter load capacitance in each of the pump stages to complete inverter draft is approximately given by:

$$C_{L_{inv}} \approx C_{DD_{Mp}} + C_{DD_{Mn}} + C_{GG_{Ms}}, \qquad (2)$$

where $C_{DD_{Mp}}$ is a drain capacitance of the M_p transistor, $C_{DD_{Mn}}$ is drain capacitance of the M_n transistor and $C_{GG_{Ms}}$ is gate capacitance of the switch transistor M_s in (F). Because $t_{HL} > t_{LH}$ as the consequence of the inverter draft [6], thus the fall time is *decisive* for PMOS transistor sizing.

The algorithm that finds the number of pump stages N represents the computationally the most demanding part of the complete procedure, see Fig. 2. It consists of three basic steps: *generating of the state equations for N-stage charge pump model [11], calculation of the time response characteristics of the pump output voltage $v_z(t)$ at given number of the pump stages $\hat{N}_i$ and evaluation of the results and estimation of the new pump stages $\hat{N}_{i+1}$.* The initial number of the stages is set based on the input parameter values - *output voltage and load current, ripple voltage and clock signal frequency* for analysis algorithm via to **state-space model**. The following equation comes from the theoretical relationship [2], which is modified for the BSIM model:

$$\hat{N}_{i_0} = \text{round} \cdot \ldots$$
$$\cdot \left(\frac{R_L C f_{clk} \alpha \beta \rho}{2C^2 R_L V_{DD} f_{clk} - 2V_{out,av} (C + C_{mont})} \right), \qquad (3)$$
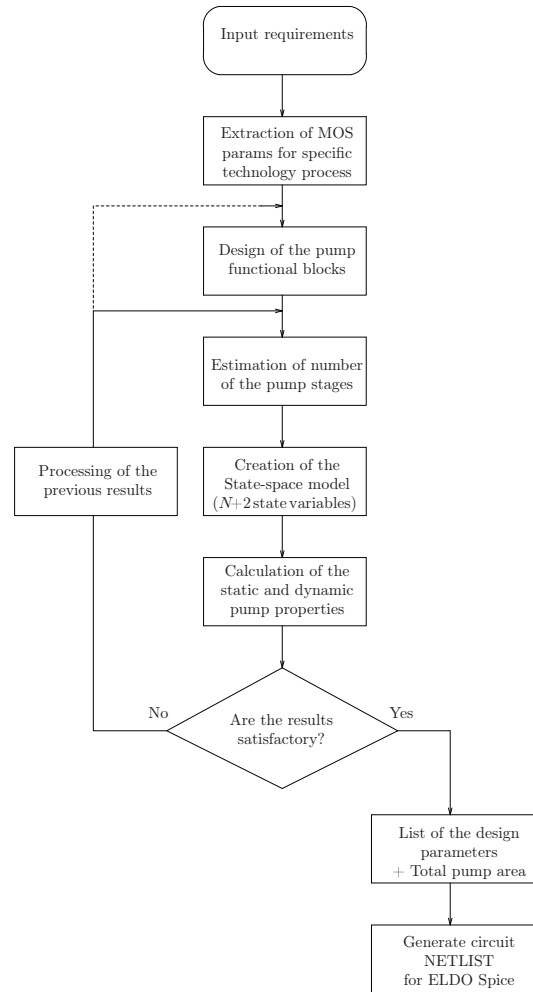

Fig. 2: Basic principle of the charge pump synthesis algorithm.

where:

$$\alpha = (C + C_{mont}) \cdot \ldots$$
$$\cdot (K_{1ox}\sqrt{4\phi_s + 2V_{r\,max}} - 2K_1\sqrt{\phi_s}), \qquad (4)$$

$$\beta = C(K_{2ox}V_{r\,max} + 2V_{out,av} - 2V_{DD} + 2V_{TH0}), \quad (5)$$

$$\rho = C_{mont}(K_{2ox}V_{r\,max} + 2V_{out,av} + 2V_{TH0}), \qquad (6)$$

where R_L is load resistance in (Ω), C is main capacitor and C_{mont} is added strange capacitor value (see Fig. 1) in (F), f_{clk} is clock signal frequency in (Hz), V_{DD} is power supply voltage, $V_{out,av}$ is average value of the output voltage, $V_{r\,max}$ is ripple of the output voltage and V_{TH0} is threshold voltage of NMOS at zero bias voltages in (V), ϕ_s is surface potential in (V) and K_1, K_{1ox}, K_{2ox} are body effect coefficients in (-) [7]. Equation expressing the relationship between the output voltage and the number of stages is well- known from SC circuit theory but its form for the BSIM MOSFET model has not been published yet. Equation (3) does not provide the correct result in the vast majority of cases, the reasons of this are explained in detail in [1], [2], [4] and [5], thus in real $N > \hat{N}_{i_0}$.

In the next step, the procedure automatically generate set of the first order differential equations with initial conditions [11], which describe the behaviour of the N_i-pump stage model for each phase $(\phi, \bar{\phi})$ of the clock signal (analogue domain). Philosophy of the analysis part including an estimation of some static and dynamic characteristics is listed in [11]. Initial conditions for the next phase [11] (digital domain) is complemented by other findings. If the nonlinear-capacitors are used, then its capacitance is jump changed at the beginning of the next phase. The initial value of the i-state variable is given by:

$$v_{C_{i_0}}^{(k+1)} = \text{sgn}_{V_{DD}} V_{DD} \cdot \dots$$

$$\cdot \frac{C_{s_i}^{(k+1)}(v) + C_{mont}}{C_i^{(k+1)}(v) + C_{s_i}^{(k+1)}(v) + C_{mont}} + v_{C_i}^{(k)}|_{t=k \cdot T_{clk}/2}, \tag{7}$$

where $C_{(s)i}^{(k+1)}(v)$ labels instante capacitance value in (F) at bias voltages, which correspond to the voltage values at the end of the previous phase and this state variable value at the time $T_{clk}/2$ increased by the clock voltage level V_ϕ, $V_{\bar{\phi}}$ of the actual voltage level:

$$C_{(s)i}^{(k+1)}(v) = \dots$$

$$\begin{cases} C_{(s)i}^{(k)}|_{v, v_{ci}^{(k)} + \max\{V_\phi, V_{\bar{\phi}}\}}, & \text{for active interval} \\ C_{(s)i}^{(k)}|_{v, v_{ci}^{(k)} + \min\{V_\phi, V_{\bar{\phi}}\}}, & \text{for passive interval} \\ \text{and } t = k \cdot T_{clk}/2, & k \in \{1, 2, ..., n\}, \end{cases}$$
$$\tag{8}$$

where k expresses the multiple of the half of the clock signal period and $sgn_{V_{DD}}$ is equal to $+1$ for passive, -1 for active interval respectively [11]. When one of the M_d transistors becomes from strong inversion region to subthreshold region (considering $I_D = 0$ in the model) during the active interval of CLK while the switch transistor is OFF, then the end value at $kT_{clk}/2$ is corrected according to the equation:

$$v_{C_{i_0}}^{(k+1)\prime} = v_{C_{i_0}}^{(k+1)} + |V_{OFF}|, \tag{9}$$

where V_{OFF} is model parameter (cut-off voltage) in (V). The same is applied if the bias voltage of the switch transistor $v_{DS} = v_{GS}$.

Calculation of the state variables, which also include output voltage, is similar to the principle of *state machine*. The process is ended in the steady state, this is detected mainly based on *icreasing of the voltage gain in time [10], depending on the shape of the function of the output voltage and from evaluating of the previous time response(s) (if they have already been implemented)*. Providing the output voltage V_{z_i} does not reach the required level $V_{out,av}$, the number of the stage for next iteration, labelled $\hat{N}_{i+1}$, is estimated from *Lagrange's polynomial function* and the procedure is repeated.

The algorithm checks the state of all the transistors during computing and reports that correct functionality of the circuit is not guaranteed. This can occur, for example, if the maximum number of the pump stages is exceeded (the task has no solution) or the output voltage decreases with the number of stages, etc. When the synthesis process is ended, the list of design parameters is displayed and the system generates a circuit netlist with calculated elements values for ELDO Spice and estimates the pump area on chip according to the equation:

$$S_{pump} \approx 1.3 \left[N(W_n L_n + W_p L_p + W_s L_s) \right] + \dots$$
$$+ 1.3 \left[(N+2)(W_d L_d) + (N+1) W_c L_c \right], \tag{10}$$

where W_c, L_c are MOS capacitor sizes and constant 1.3 becomes from practical design - about 30 % of the total components area is reserved for routing on the layout.

3. Experimental Part

The following application of the voltage converter can be used as a secondary power block which increases the clock signal amplitude of the main charge pump. It greatly improves the voltage efficiency of the main pump that operates at the low supply voltage. Input requirements are listed in Tab. 1.

Tab. 1: List of the input pump requirements.

Output voltage	$V_{out,av}$	$\geq$ 3.3 V
Output load current (max.)	$I_{L\max}$	$\leq$ 0.6 µA
Maximal outptut ripple voltage	$V_{r_{\max}}$	$\leq$ 2 mV
Power supply voltage	V_{DD}	0.8 V
Clock signal amplitude	V_ϕ	0.8 V
Clock signal frequency	f_{clk}	10 MHz

The topology consists of MOS capacitors, added parasitic impedance in the nodes are not considered. The step involving the pump block design in according to the hierarchy from Fig. 2 will be skipped. It was shown in [3], [6] and [8]. Initial value of N in according to Eq. (3) is set to $N_{i0} = 3$, this corresponds to the calculated output voltage of 2.44 V in steady state. In the end, three iterations of N are performed to achieve a voltage level 3.3 V. Output voltage function of N is described by the following equation:

$$\hat{V}_{out,av}(N) \approx \begin{cases} 0.15N + 1.99, & \text{for } 3 \leq N \leq 5, \\ 0.56N, & \text{for } N \geq 6, \end{cases}$$
$$\tag{11}$$

where N is the integer. An illustration of the programme report is listed below.

The estimation of the pump output voltage in according to Eq. (11) was also verified in ELDO Spice. A comparison of the calculated and simulated pump

Number of N iterations: 3.

Total number N stages: $N = 6$.

Average value of the pump output voltage: V_{outav} = 3.4039 V.

Ripple value of the pump output voltage: V_r = 1.8 mV.

Relative error of the output voltage: E_r = 3.15 percent.

Rise time of the output voltage: T_r = 7.15 μs.

Fig. 3: Report if the results in Maple software.

output voltage values at each step of the procedure, when the new value of $\hat{N}$ is set by the design algorithm, is given in Tab. 2. The value of the "STATUS" flag indicates whether the desired output voltage has been reached. If $\hat{V}_{out,av} \geq V_{out,av,desired}$, then STATUS flag is set to "1" and the iteration process is stopped. The data from Tab. 2 also show that synthesis without using of the design algorithm does not provide satisfactory results because the pump with $N = 3$ calculated from Eq. (4) gives output voltage only 2.44 V . The number of stages is actually twice of the theoretical value.

Tab. 2: Comparison of the estimated and simulated output voltage values with N.

		Algorithm	ELDO	
iter.	$\hat{N}$ (-)	$\hat{V}_{out,av}$ (V)	$V_{out,av}$ (V)	STATUS
1	3	2.44	2.48	0
2	5	2.74	2.76	0
3	6	3.36	3.45	1

Finally, statement of the draft results is shown in Tab. 3.

Remark 1. *Rise time is defined as the time, in which the time response characteristic intersects 70 % of the maximum value in the steady state [4], i.e. $v_z|_{t=T_r} = 0.7\ V_{out,av} = 2.31$ V for this example. The pump dynamic properties are evaluated especially in the beginning of the charge transport at $t = 0$, when the clock signal is connected to the pump circuit with zero internal node voltages. When the time output characteristic approaches the steady state, the change of circumferential quantities (charge currents, voltage gain) is very small. Pump voltage gain sharply declines over time, thus the total time required to reach the 100 % of the steady state value can be much longer than rise time.*

Calculated time response characteristics of the six-stage charge pump output voltage compared to simulation results in ELDO is shown in Fig. 4.

The static and dynamic properties were analyzed for various clock signal frequency changes, while the other pump parameters were retained according to Tab. 3. The purpose of the analyzes is to verify the validity if the optimization process. As it follows from Fig. 2, the pump output voltage (average value) acquires the required voltage level over a wide frequency range

Tab. 3: Composition of red-emitting $Sr_wF_xB_yO_z$:Eu^{2+}, Sm^{2+} phosphor.

| Conditions		
Temperature	ϑ	22 °C
Model of MOSFETs M_d, M_s, M_n: *nmos_ hvt*		
Model of MOSFETs M_p: *pmos_ hvt*		
Model of MOSFETs M_c: *nmos_ nat*		
MOS corner analysis: *Typical*		
Design parameters		
Number of stages	N	6
Main capacitor value	C	6.5 pF
MOSFETs sizing		
Channel length of M_D,M_s, M_p, M_n	L	1 μm
Width of M_d: nmos_ hvt	W_{Md}	31.5 μm
Width of M_s: nmos_ hvt	W_{Ms}	0.6 μm
Width of M_p: pmos_ hvt	W_{Mp}	1 μm
Width of M_n: nmos_ hvt	W_{Mn}	11 μm
MOS capacitor sizing - nmos_nat		
Channel length	L_c	14 μm
Channel width	W_c	137 μm
Pump stage area	S_{stage}	1963.1 μm²
Total pump area on layout (est.)	S_{pump}	0.018 mm²
Estimation of static and dynamic parameters		
Output voltage (avg.)	$\hat{V}_{out,av}$	3.36 V
Output ripple peak voltage	$\hat{V}_r$	1.8 mV
Rise time 1	$\hat{T}_r$	7.15 μs
Static voltage efficiency	$\hat{\eta}_v$	57 %
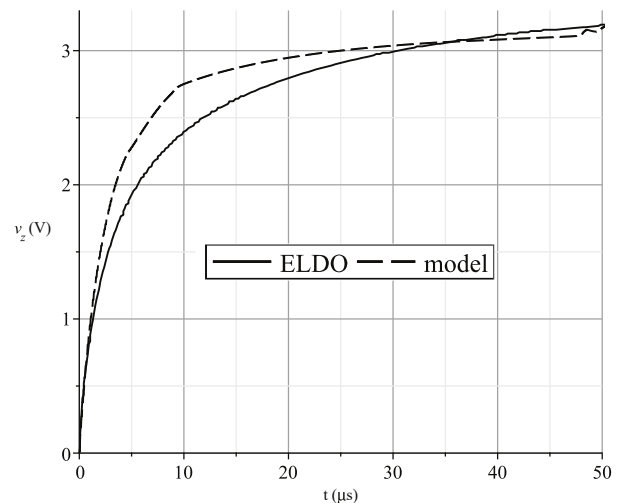
Fig. 4: Time response characteristic of the six-stage pump output voltage.

0.1–100 MHz. The relative deviation from the maximum voltage value is less than 2 % at frequency $f = 10$ MHz, see Fig. 5. Low sensitivity of the output voltage to the change in capacitance values is therefore guaranteed. This property is necessary for practical design in view of the nonlinear character of the MOSFET capacitors.

The dependence of the pump dynamic properties - rise time on the clock frequency is shown in Fig. 6. The time was detected at the voltage level $V_{fin} = 2.31$ V for each of time response characteristic with different CLK frequency. The relationship $T_r \sim \frac{1}{f_{clk}}$ is valid
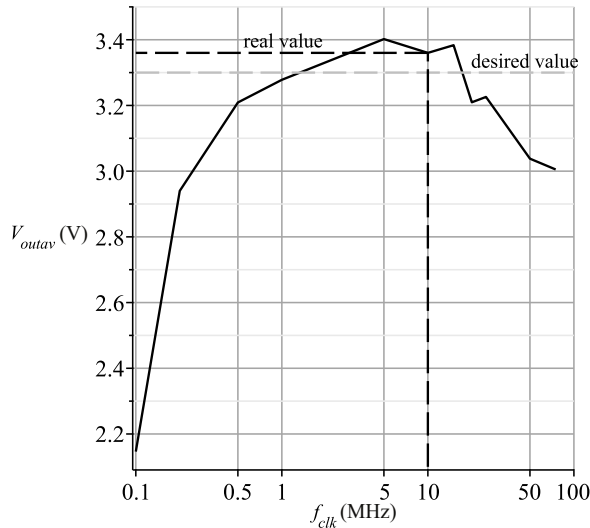
Fig. 5: Pump output voltage vs clock signal frequency.

for this example (it cannot be generalized for arbitrary pump design circuit). Pump propeties for the various clock frequncy changes are summarized in Tab. 4.

Remark 2. *The final required value V_{fin} was not exceeded for this frequency.*

However, the solution may not (and usually not) be optimal for another clock signal frequency despite the fact that the output voltage requirement is fulfilled. Afterthat, the proposal should be revised, so that the main design criteria - maximal voltage gain was fulfilled.

Example 1. *The pump draft will be made at the same conditions, as it is shown in Tab. 1 but clock frequency $f_{clk} = 20$ MHz will be considered in order to reduce the rise time.*

*Using the synthesis algorithm, the recalculated MOSFETs sizing are: $L = 1$ μm, $W_{M_d} = 14$ μm, $W_{M_s} = 3.7$ μm. Other components (C, W_{M_p}, W_{M_n}, ...) remain unchanged. **The new pump has only 4 stages.** Simulated selected pump properties with N iterations are summarized in the following Tab. 5. The main benefit of the recalculation is higher static eficiency (it was about 57 % before recalculation according to Tab. 4 and now it is about 83 % at frequency $f = 20$ MHz), while keeping the minimal output voltage level 3.3 V.*

Production cost minimization is an important part of the proposal in practice. It means the voltage gain may not be decisive from an economic point of view. The charge pump final version is most often designed to *minimize the area on a chip* (layout topology, the circuit parameters). The main capacitor C always represents the circuit element with the largest area in comparison with others elements in the pump stage, as
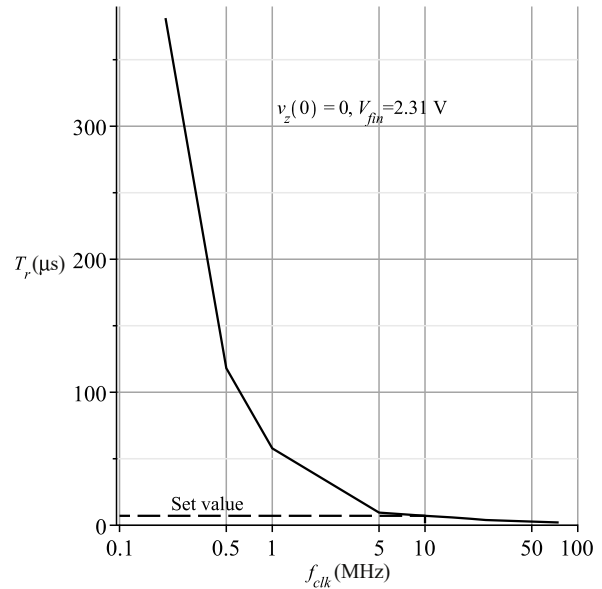

Fig. 6: Rise time vs clock signal frequency.

Tab. 4: Simulated static and dynamic properties of the six-stages charge pump with the clock frequency changes.

f_{clk} (MHz)	$V_{out,av}$ (V)	V_r (mV)	T_r (μs)
0.1	2.15	159	X (Rem. 2)
0.2	2.94	74	381.3
0.5	3.21	32.2	118.1
1	3.28	15.9	57.8
5	**3.40**	**3.6**	**9.5**
10	**3.36**	**1.8**	**7.1**
15	**3.38**	**1.2**	**5.9**
20	3.21	0.9	4.9
25	3.23	0.7	3.9
50	3.04	0.5	2.8
75	3.00	0.4	2.1

Tab. 5: Simulated static and dynamic properties of the charge pump for $f_{clk} = 20$ MHz.

N (-)	$V_{out,av}$ (V)	V_r (mV)	T_r (μs)
3	2.82	1.4	3.00
4	**3.52**	**1.4**	**3.01**

it follows from Tab. 3. Decreasing the main capacitor means that the pump must have more stages to achieve the same output voltage level. However, increasing of the number of the pump stages does not always mean that output voltage will grow to the desired value (task does not have a solution in extreme case). The algorithm in Fig. 7 is designed to find a relationship between the number of stages and main capacitor value so that the pump state area is minimal and the pump losses (switch reverse current and inverter cross current) in each of the pump stages were at the lower limit. Procedure in Fig. 7 starts from solution for optimization of the pump voltage gain. Pump consists N_g number of stages and main capacitors value C_g. The procedure firstly selects pair W_i and $C_i < C_g$
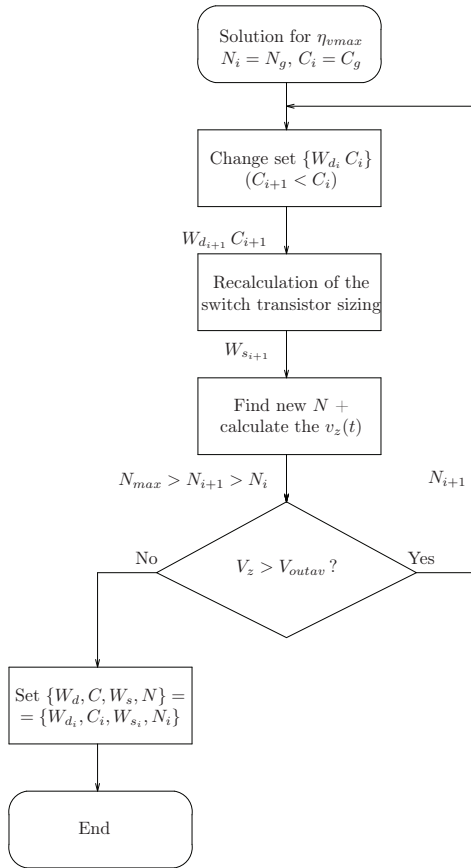
Fig. 7: Algorithm for pump area optimization.

from the solutions set of equations [8]:

$$v_c|_{t=T_{clk}/2} = \alpha \cdot v_{c_\infty}|_{V_\Phi=0}, \qquad (12)$$

$$v_z(W_{MD}, C)|_{t=nT_{clk}/2} \geq V_{out,av} + \frac{V_r}{2}, \qquad (13)$$

where the meaning of the symbols is explained in [8] and subsequently recalculates the switch transistor sizing. After that, the analysis algorithm tries to find the new number of stages, labelled $N_i(> N_g)$, according to the procedure in Sec. 2. . If the solution exists, the new pair $\{W_{di+1}, C_{i+1}\}$ is selected and the process is repeated until the output voltage $\bar{V}_z$ is less than $V_{out,av}$. The number of stages is the critical parameter in this case. Considering the set of the input parameters from Tab. 1, possible pairs of solution Eq. (13) - transistor width in µm and main capacitor value in (pF) are: $[W_d, C] = \{[1, 0.5], [4.5, 1.5], [10, 2.5], [15.5, 3.5], [21, 4.5], \dots\}$. The result in according to algorithm from Fig. 7 satysfying the conditions $\bar{V}_z > V_{out,av}$, $N < N_{\max} = 20$ and minimal capacitance value is $\{W_{sopt,a} = 0.5, \text{µm}, W_{opt,a} \, C_{opt,a}\} = \{10, 2.5 \, \text{pF}\}$ for $N = 14$. MOS capacitor sizing is $W_c = 72.1$ µm and $L_c = 10$ µm. Sizing of the other components is the same, see Tab. 3.

Total charge pump area calculated from Eq. (10) is 0.0145 mm² is about **20** *% less than in the previous case, see Tab. 3. The pump voltage efficiency is only about* **27** *%.*

4. Conclusion

The utility for the design of the cross-coupled charge pump was discussed in this article. Synthesis process, which is the result of the current research in the field of two-phase charge pumps, significantly facilitates designer's work. The algorithm is based on the pump elementary blocks modelling through the symbolic description by using the BSIM model description. Sizing of the pump components is derived from both the static (CMOS inverter) and state equations (switch transistor, main capacitor sizing, etc.) from and solving of the state equations, which meet the prerequisites following from continuous pump character during the phase of the clock signal. Pump stage model including both the static and dynamic equations reflects dominant pump real effects (threshold voltage and body effect, bulk charge effect, substrate capacitances, . . .). Subblocks were designed, so that the pump voltage static efficiency is maximal, see Eq. (1). Complex model is used for calculating the number of pump stages in the synthesis process through the state-space description, as it is shown in Fig. 2. The number of stages for computing cycle is estimated by using the *Lagrange's* interpolation polynomial function, initial $1N$ was calculated from Eq. (4). The full mentioned process was shown in the practical example, in which the pump design was done based on both the maximal static efficiency and minimal total pump area. If the theoretical Eq. (4) is used for the the charge pump design without this algorithm, the relative error of the output voltage is about 25 %. On contrary, the procedure provides results with relative error of the output voltage about 3 %. The validity of the optimization process and predicted pump properties were verified by simulations in ELDO, as it was shown in Fig. 5, Fig. 6 and Tab. 4, Tab. 5. Comparision between the calculated and analysis time response characteristic shows Fig. 4.

The procedure allows, among other functions, to generate *netlist for ELDO* and estimate the total pump area, see Eq. (10). Description approach is complicated and allows to observe a number of static and dynamic parameters with acceptable accuracy. On the other hand, some dynamic properties, as power dissipation cannot be calculated because of the neglecting of the transition between phases of CLK and other effects cited in [4] and [5].

Future work will be focused on creating a graphical interface for the design utility, pump draft in the corners, as SS, FF and comparison of the design pa-

rameters with the results of optimization (numerical) algorithm.

Acknowledgment

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About Authors

Jan MAREK was born in Prague on April 8, 1990. He graduated from the Czech Technical University in Prague in 2014 and is currently studying towards Ph.D. at the Department of Circuit Theory. His research interests deal with the design of current analog circuits, as well as their optimization.

Jiri HOSPODKA was born in 1967. He received his Master's and Ph.D. degrees from the Czech Technical University in Prague in 1991 and 1995, respectively. Since 2007 he has been working as associate professor at the Department of Circuit Theory at the same university. Research interests: circuit theory, analog electronics, filter design, switched-capacitor, and switched current circuits.

Ondrej SUBRT was born in Hradec Kralove on February 24, 1977. He works as analog design engineer with ASICentrum Prague, a company of the Swatch Group. At present, he has also been appointed an Ass. Prof. at the Faculty of Electrical Engineering, CTU Prague. His research interests being analog and mixed-signal integrated circuits design with emphasis to low-power low-voltage techniques and innovative design and verification methods of data converters.